( ) Preliminary Specification
(V) Final Specification

Module	15.6 Inch Color TFT-LCD
Model Name	G156XW01 V4

Customer	**Date**	**Approved by**	**Date**
		Sean Lin	02/09/2018
Checked & Approved by	**Date**	**Prepared by**	**Date**
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Customer's sign back page		General Display Business Division / AU Optronics corporation	

Contents

Record of Revision

Version	Date	Page	Old description	New Description
1.0	2018/02/09	All	First draft specification	

1. Operating Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
6) To avoid ESD (Electro Static Discharde) damage, be sure to ground yourself before handling TFT-LCD Module.
7) Do not open nor modify the module assembly.
8) Do not press the reflector sheet at the back of the module to any direction.
9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Severe temperature condition may result in different luminance, response time and lamp ignition voltage.
14) Continuous operating TFT-LCD display under low temperature environment may accelerate lamp exhaustion and reduce luminance dramatically.
15) The data on this specification sheet is applicable when LCD module is placed in landscape position.
16) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or shuffle content periodically if fixed pattern is displayed on the screen.

2. General Description

This specification applies to the 15.6 inch-wide Color a-Si TFT-LCD Module G156XW01 V4. The display supports the HD - 1366(H) x 768(V) screen format and 16.2M colors (RGB 6-bits+2-FRC data). All input signals are eDP(Embedded DisplayPort) interface and this module contains with an LED driver for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

Items	Unit	Specfications
Screen Diagonal	[inch]	15.6”
Active Area	[mm]	344.232 (H) x 193.536 (V)
Resolution		1366 x 768
Pixel Pitch	[mm]	0.252 x 0.252
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		TN Mode, Normally White
Nominal Input Voltage VDD	[Volt]	+5.0 (Typ.)
LCD Power Consumption	[Watt]	2.2W (Typ.), 2.6W (Max.) (all black pattern)
LED Power Consumption	[Watt]	6W (Typ.),7.2W(Max.) (all black pattern)
Weight	[g]	860 (Typ.)+/- 40
Physical Size	[mm]	363.8(W) X 215.9(H) X 9.3 (D) (Typ.)
Electrical Interface		eDP1.2
Surface Treatment		Anti-Glare, 3H
Support Color		16.2M colors (RGB 6-bits+FRC)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +60 (+60°C as panel surface temperature) -20 to +60
RoHS Compliance		Yes

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 °C(Room Temperature:

Item	Unit	Conditions		Min.	Typ.	Max.	Note
White Luminance (Center)	cd/m^2	I_{LED}=50mA (center point)		400	500		*1*
Luminance Uniformity	%	5 points		70	75	-	*2,3*
Contrast ratio	--			350	500	-	*4*
Response Time	msec	Rising Time (T_{rR})		-	6	9	*5*
		Falling Time (T_{rF})		-	2	4	
		Rising + Falling		-	8	13	
Viewing Angle	[degree]	Horizontal CR >= 10	(Right)	75	85	-	*6*
			(Left)	75	85	-	
		Vertical CR >= 10	(Upper)	70	80	-	
			(Lower)	70	80	-	
Color / Chromaticity Coodinates (CIE 1931)	--	Red x		0.578	0.628	0.678	
		Red y		0.297	0.347	0.397	
		Green x		0.282	0.332	0.382	
		Green y		0.565	0.615	0.665	
		Blue x		0.106	0.156	0.206	
		Blue y		0.025	0.075	0.125	
		White x		0.263	0.313	0.363	
		White y		0.279	0.329	0.379	
Color Gamut	%	CIE 1931		-	62	-	

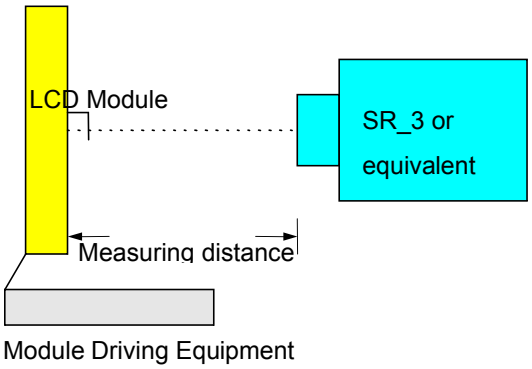
Note 1: Measurement method

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

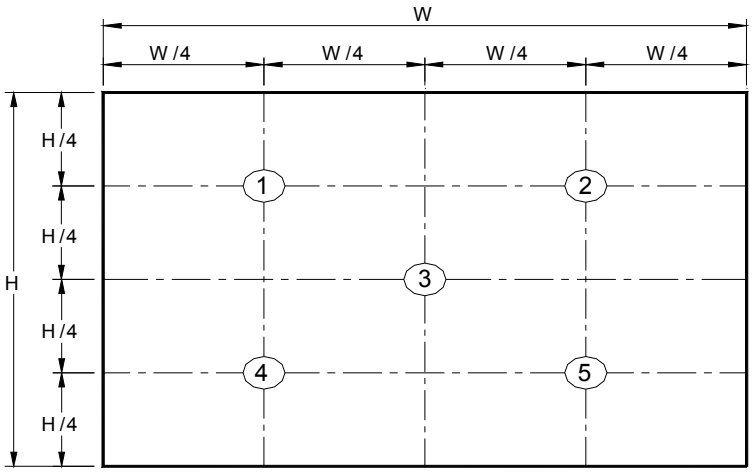
Aperture 1° with 50cm viewing distance

Test Point Center

Environment *< 1 lux*



Note 2: Definition of 5 points position



Note 3: The luminance uniformity of 5 points is defined by dividing the minimum luminance values by the maximum test point luminance

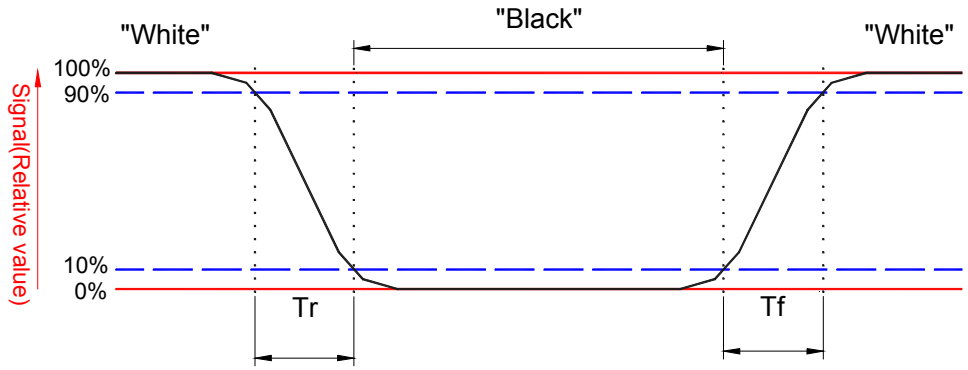
$$\delta_{W5} = \frac{\text{Minimum Brightness of five points}}{\text{Maximum Brightness of five points}}$$

Note 4: Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

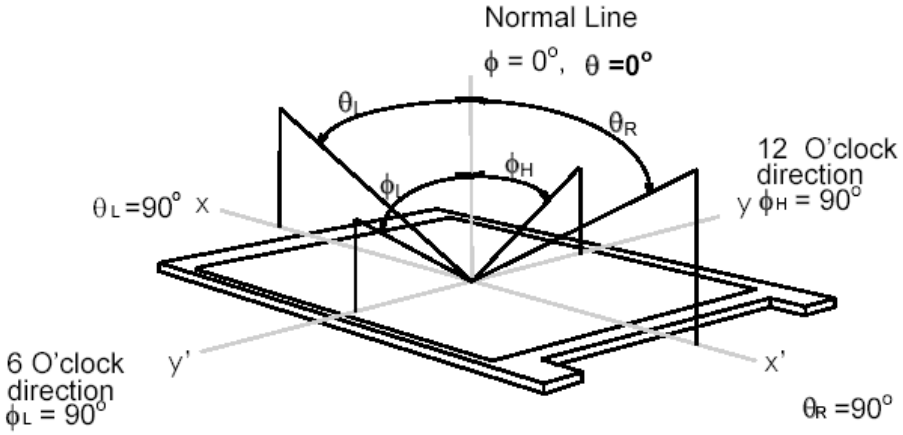
Note 5: Definition of Response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.



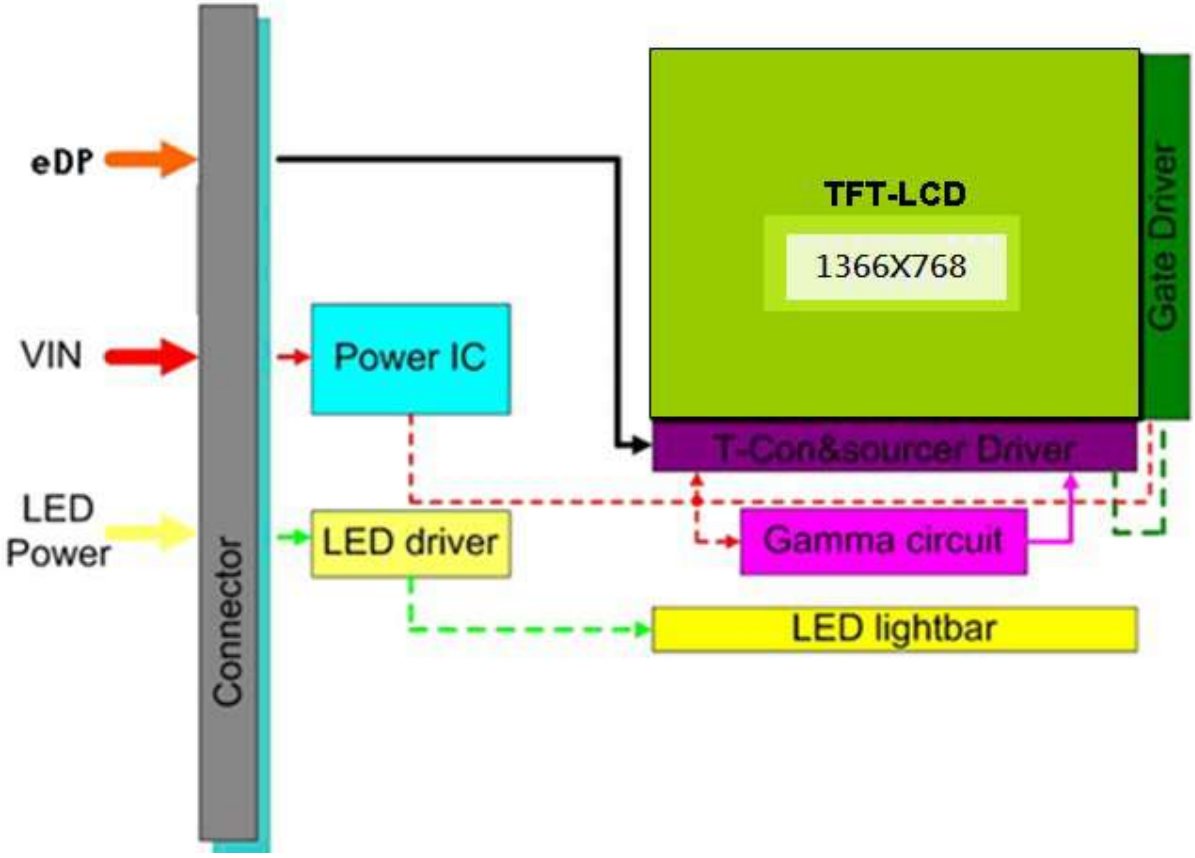
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inch Color TFT-LCD Module:



4. Absolute Maximum Ratings

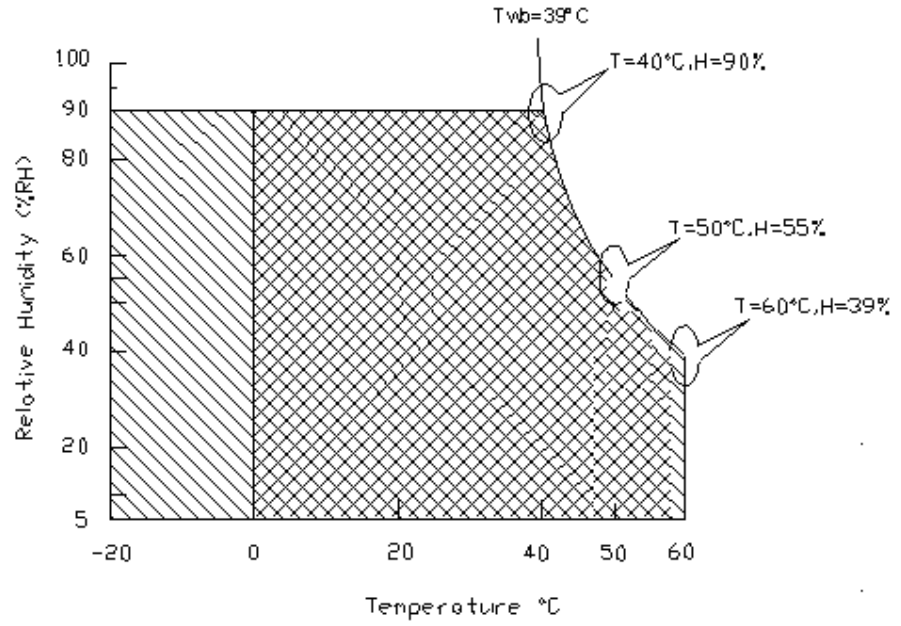
4.1 Absolute Ratings of TFT LCD Module

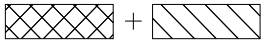
Item	Symbol	Min	Max	Unit
Logic/LCD Drive Voltage	Vin	0	6.0	[Volt]

4.2 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit
Operating Temperature	TOP	0	+60	[°C]
Operation Humidity	HOP	5	90	[%RH]
Storage Temperature	TST	-20	+60	[°C]
Storage Humidity	HST	5	90	[%RH]

Note: Maximum Wet-Bulb should be 39 °C and no condensation.



Operating Range  Storage Range 

5. Electrical characteristics

5.1 TFT LCD Module

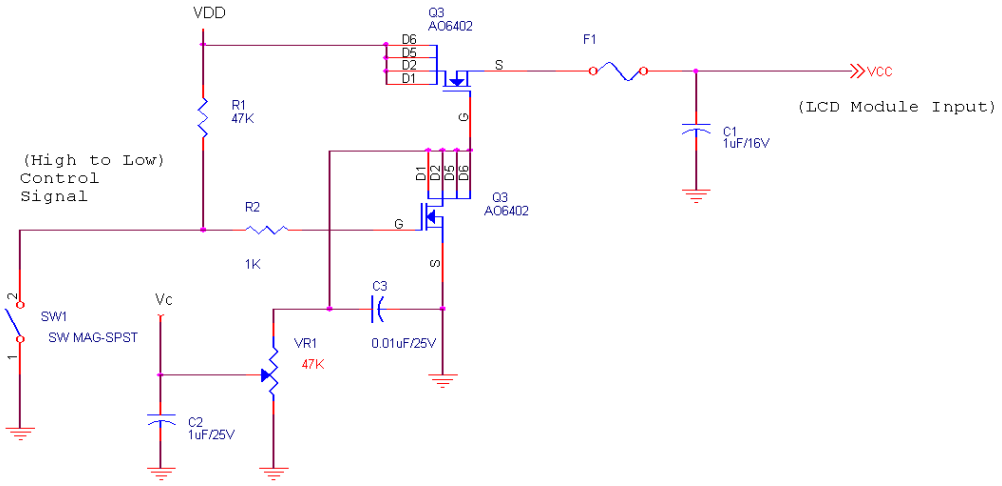
5.1.1 Power Specification

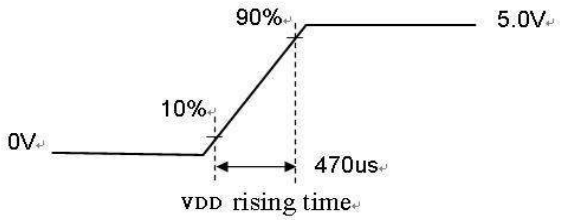
Input power specifications are as following:

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VDD	Logic/LCD Drive Voltage	4.5	5.0	5.5	[Volt]	+/-10%
IDD	VDD Current ,Input Current	-	0.43	0.52	[A]	VDD= 5.0V, All Black Pattern At 60Hz *Note 1
IRush	LCD Inrush Current	-	-	2.5	[A]	*Note 2
PDD	VDD Power	-	2.15	2.6	[Watt]	VDD= 5.0V, All Black Pattern At 60Hz
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	300	[mV] p-p	VDD= 5.0V, All Black Pattern At 60Hz

Note 1: Current fuse is built in a module. Current capacity of power supply for VDD should be larger than 2A design value, so that the fuse can be opened at the trouble of electrical circuit of module.

Note 2: Measurement conditions: The duration of rising time of power input is 470 us.

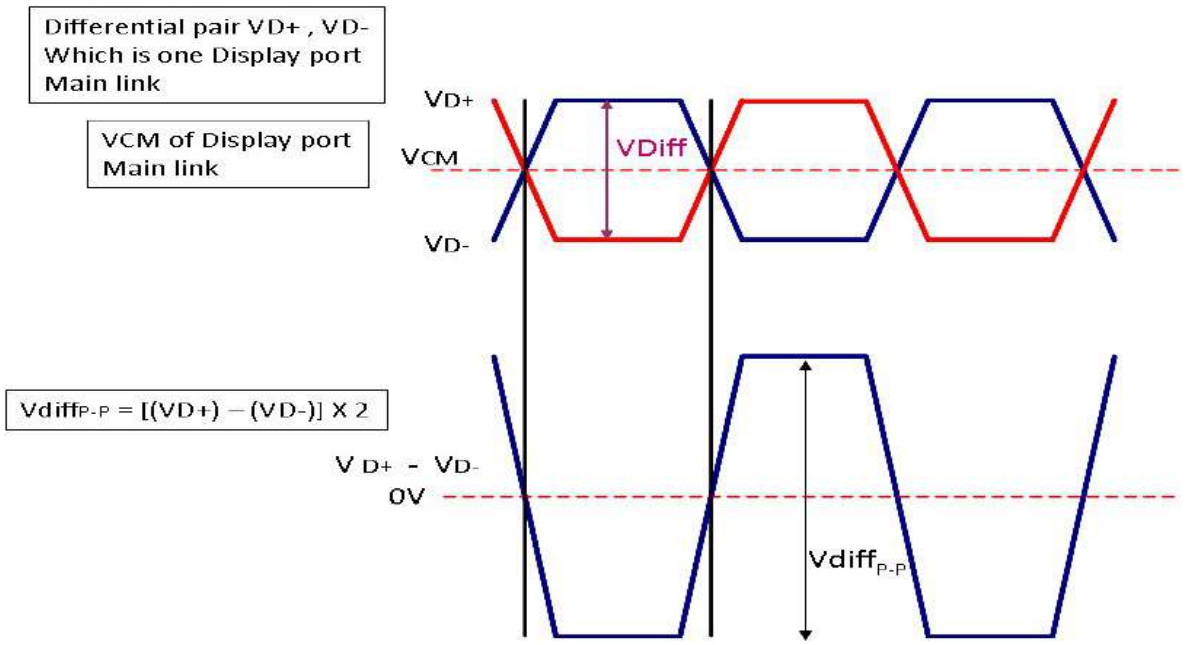




5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows:

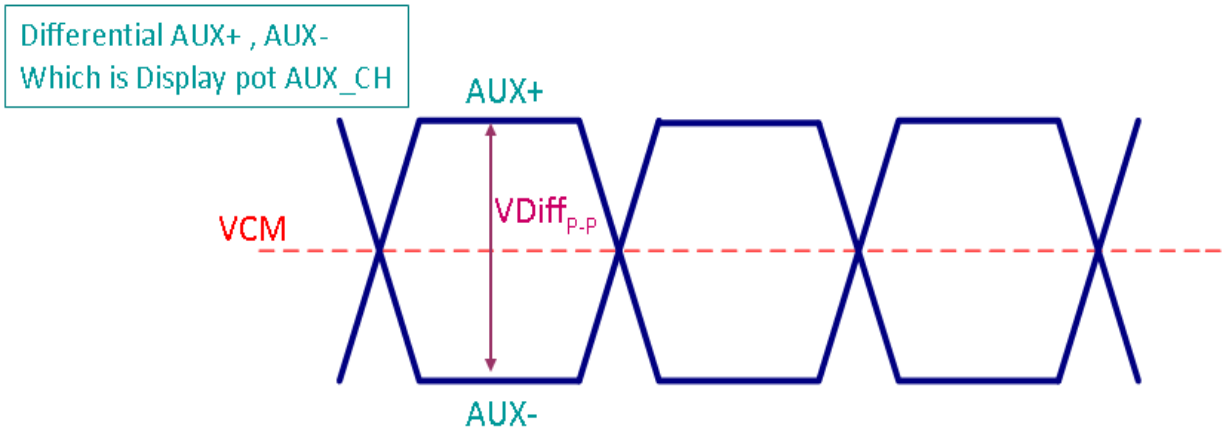
Display Port main link signal:



Display port main link					
		Min	**Typ**	**Max**	**unit**
VCM	RX input DC Common Mode Voltage		0		V
VDiff$_{P.P}$	Peak-to-peak Voltage at a receiving Device	150		1320	mV

Follow as VESA display port standard V1.1a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6-	0.8	V

Follow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	2.75	V

Follow as VESA display port standard V1.1a.

5.2 Backlight Unit

Following characteristics are measured under stable condition using a LED driving board at 25℃ (Room Temperature).

Symbol	Parameter	Min	Typ	Max	Units	Remark
VLED (Note 1)	LED Power Supply	10.8	12	13.2	[Volt]	Define as Connector Interface (Ta=25℃)
VLED_EN	LED Enable Input High Level	2.5	--	5.5	[Volt]	
	LED Enable Input Low Level	--	--	0.5	[Volt]	
VPWM_EN	PWM Logic Input High Level	2.5	--	5.5	[Volt]	
	PWM Logic Input Low Level	--	--	0.5	[Volt]	
FPWM	PWM Input Frequency *1	200	--	20K	Hz	
Duty	PWM Duty Ratio	5	--	100	%	
Ivcc	Input Current	-	0.5	0.6	A	100% Dimming
PLED	Power Consumption	-	6	7.2	Watt	
Operating Life		50000	-	-	Hrs	Ta = 25°C

Note 1: Measured on panel VLED ; Ta means ambient temperature of TFT-LCD module.

Note 2: I_F are defined for one channel LED. There are four LED channel in back light unit.

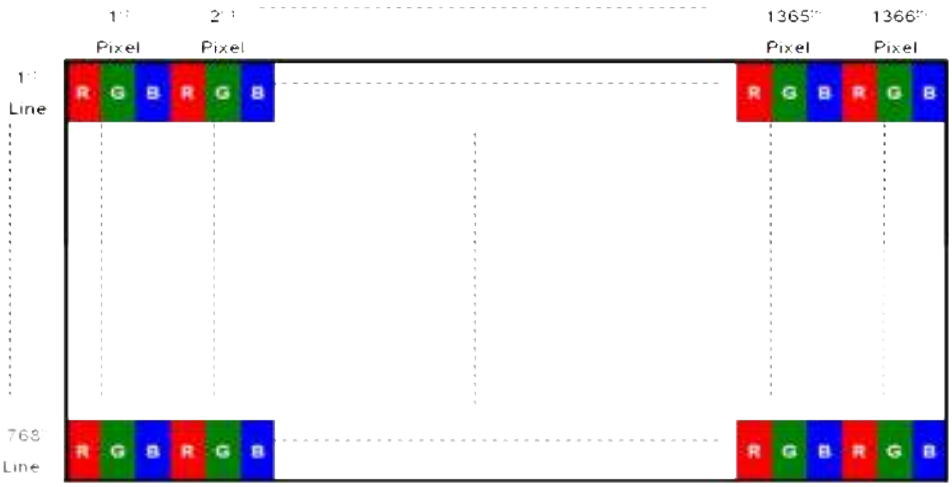
Note 3: Calculator value for reference PLED = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 4: The LED life-time define as the estimated time to 50% degradation of initial luminous at Ta = 25oC.

6. Signal Characteristic

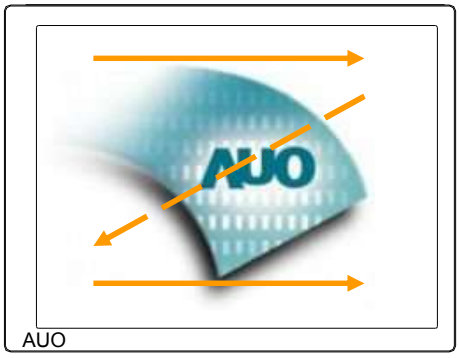
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Scanning Direction

The following figures show the image seen from the front view. The arrow indicates the direction of scan.



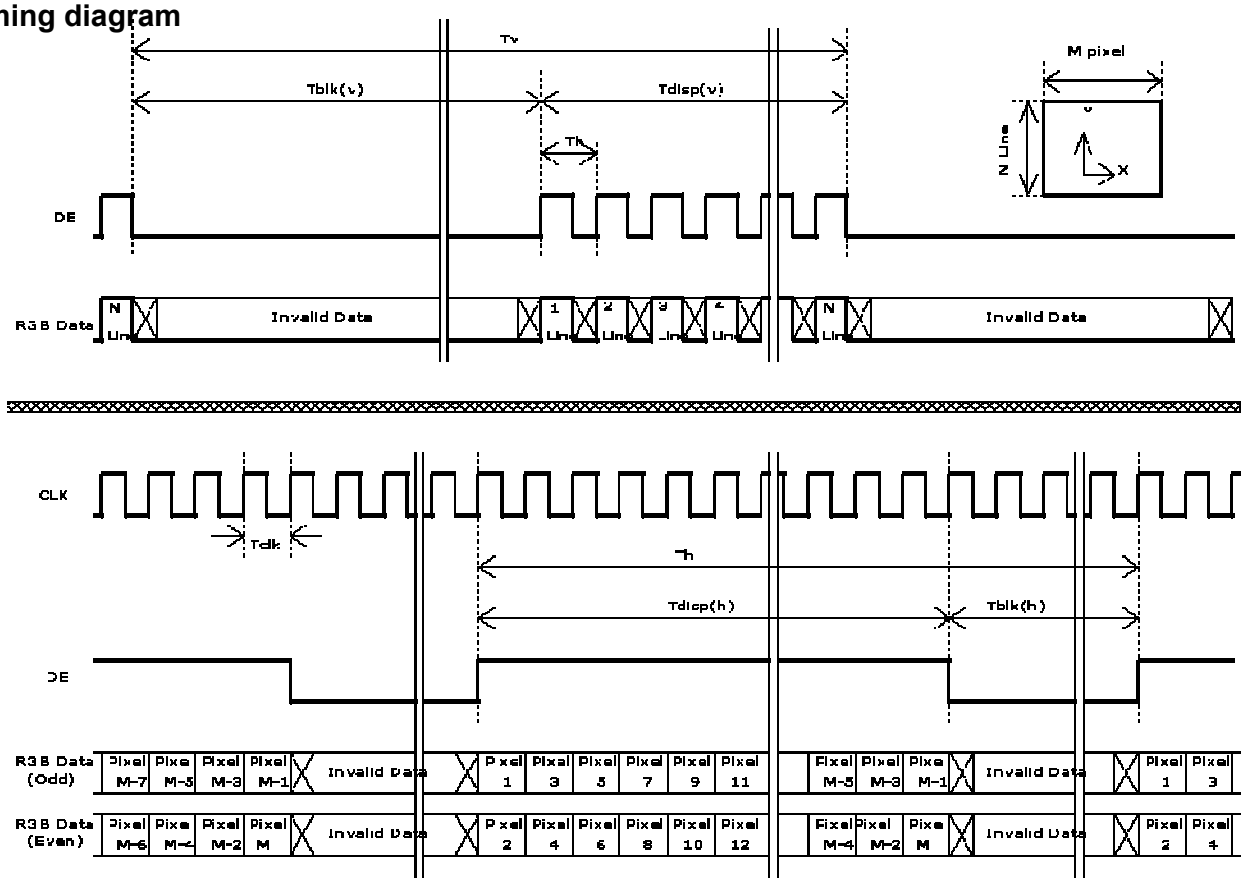
6.3 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		F	-	60	-	Hz
Clock frequency		1/ T_{Clock}	50	72.8	77	MHz
Vertical Section	Period	T_V	783	806	968	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	15	38	200	
Horizontal Section	Period	T_H	1466	1506	1866	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	100	140	500	

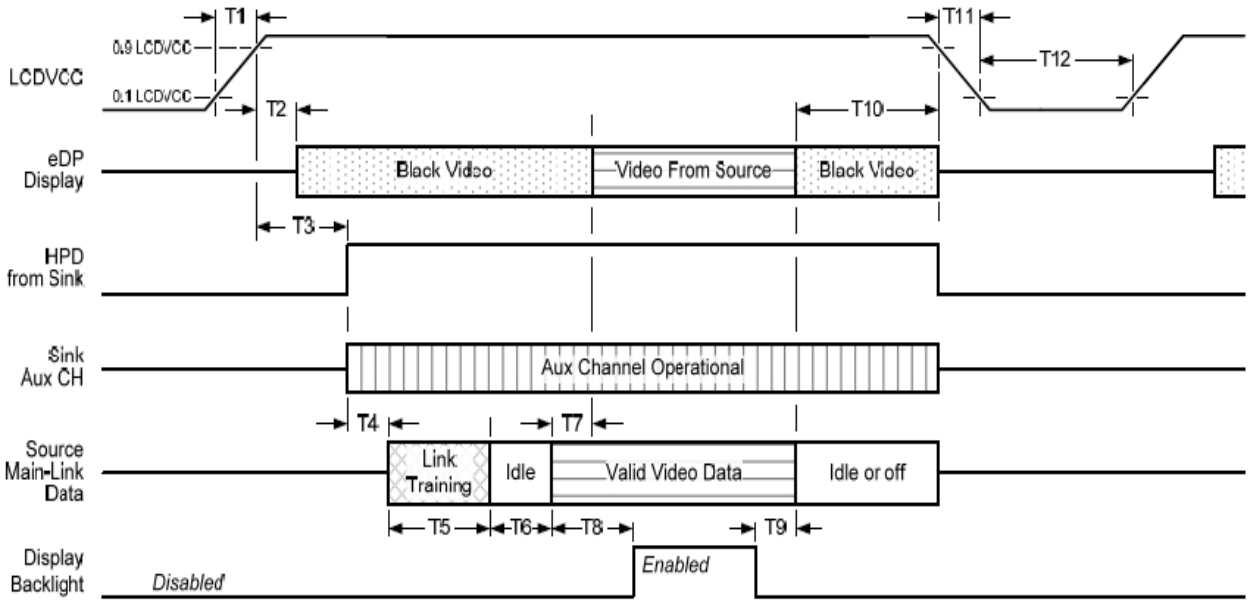
- **Note 1 :** The maximum Frame Rate < 77 MHz / [(V_Period)*(H_Period)
- **Note 2 :** Support DE mode only.
  Note 3 : Typical value refer to VESA STANDARD

Timing diagram



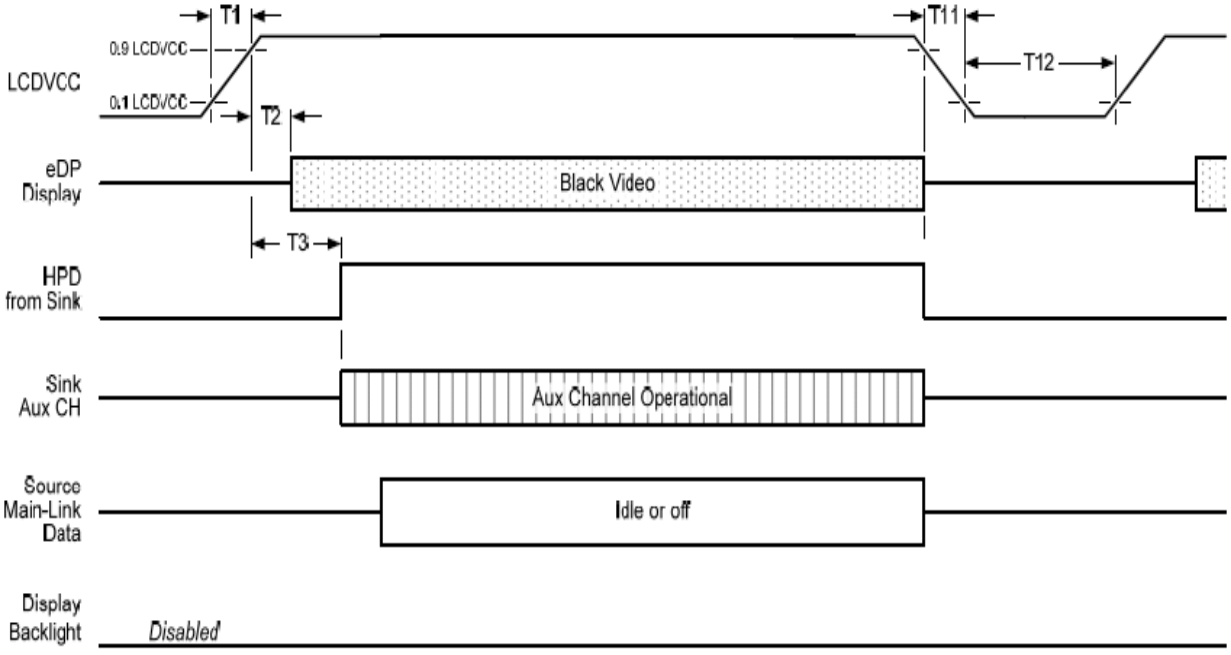
6.4 Power ON/OFF Sequence

☐**Display Port panel power sequence:**



Display port interface power up/down sequence, normal system operation

▫ **Display Port AUX_CH transaction only:**



Display port interface power up/down sequence, AUX_CH transaction only

▫ Display Port panel power sequence timing parameter:

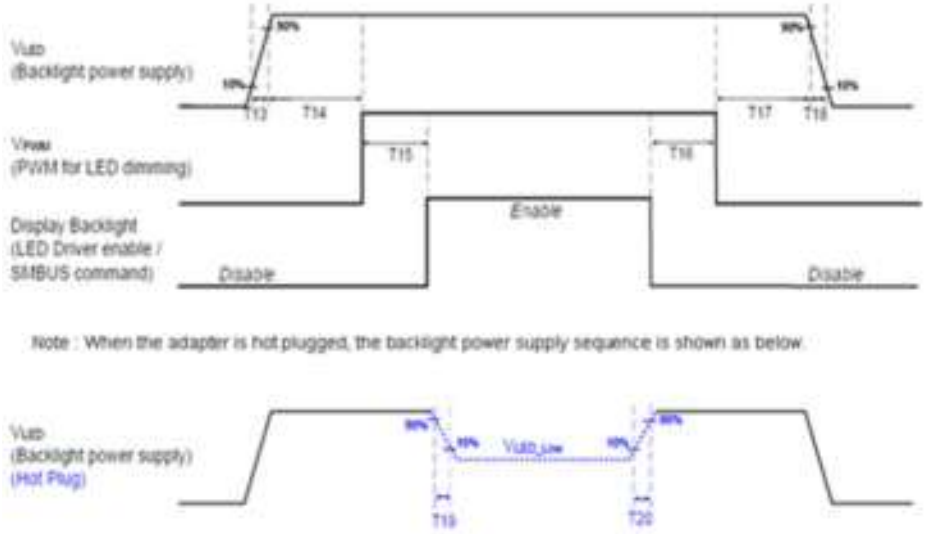
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			200ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

□ **Display Port panel B/L power sequence timing parameter:**



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	-	-
T18	-	200
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*
*T_{PWM}= 1/PWM Frequency

6.5 Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

6.5.1 TFT-LCD Signal: eDP Interface

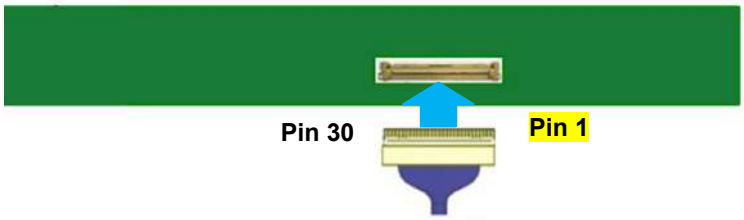
Connector Name / Designation	Interface Connector / Interface card
Manufacturer	IPEX or Compatible
Type Part Number	IPEX 20455-030E-12 or Compatible
Mating Housing Part Number	IPEX 20453-030T-11 or Compatible

6.5.2 Pin Assignment

The module input signal is eDP 30 pin, and the input eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN No.	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	NC	Not used (eDP Lane 1)
4	NC	Not used (eDP Lane 1)
5	H_GND	High Speed Ground
6	Lane0_N	True Signal Link Lane0
7	Lane0_P	Comp Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	NC	No connect
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	NC	No connect
25	NC	No connect
26	BL_PWR	Backlight power (10.8V~13.2V)
27	BL_PWR	Backlight power (10.8V~13.2V)
28	BL_PWR	Backlight power (10.8V~13.2V)
29	BL_PWR	Backlight power (10.8V~13.2V)
30	NC	No Connect

Connector Illustration



Note1: Pin1 start from right side of connector.

Note2: Input signals shall be low or High-impedance state when VDD is off.

7. Reliability Test Criteria

☐ Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50 °C, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 60 °C, 300hours, For panel surface temp.	
Low Temperature Operation (LTO)	Ta= 0 °C, 300hours	
High Temperature Storage (HTS)	Ta= 60 °C, 300hours	
Low Temperature Storage (LTS)	Ta= -20 °C, 300hours	
Thermal Shock Test (TST)	-20 °C /30min, 60 °C /30min, 100 cycles	
Hot Start Test	60 °C /1 Hr min. Power on/off per 5 minutes, 5 times	
Cold Start Test	-20 °C /1 Hr min. Power on/off per 5 minutes, 5 times	
Shock Test (Non-operation)	50G,20ms,Half-sine wave,(+-X,+-Y,+-Z)	
Vibration Test (Non-operation)	1.5G, 10~200~10Hz, Sine wave 30mins/axis, 3 direction (X, Y, Z)	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD	Contact : ± 8KV/ operation, Class B Air : ± 15KV / operation, Class B	Note 1
EMI	30-230 MHz, limit 40 dBu V/m, 230-1000 MHz, limit 47 dBu V/m	

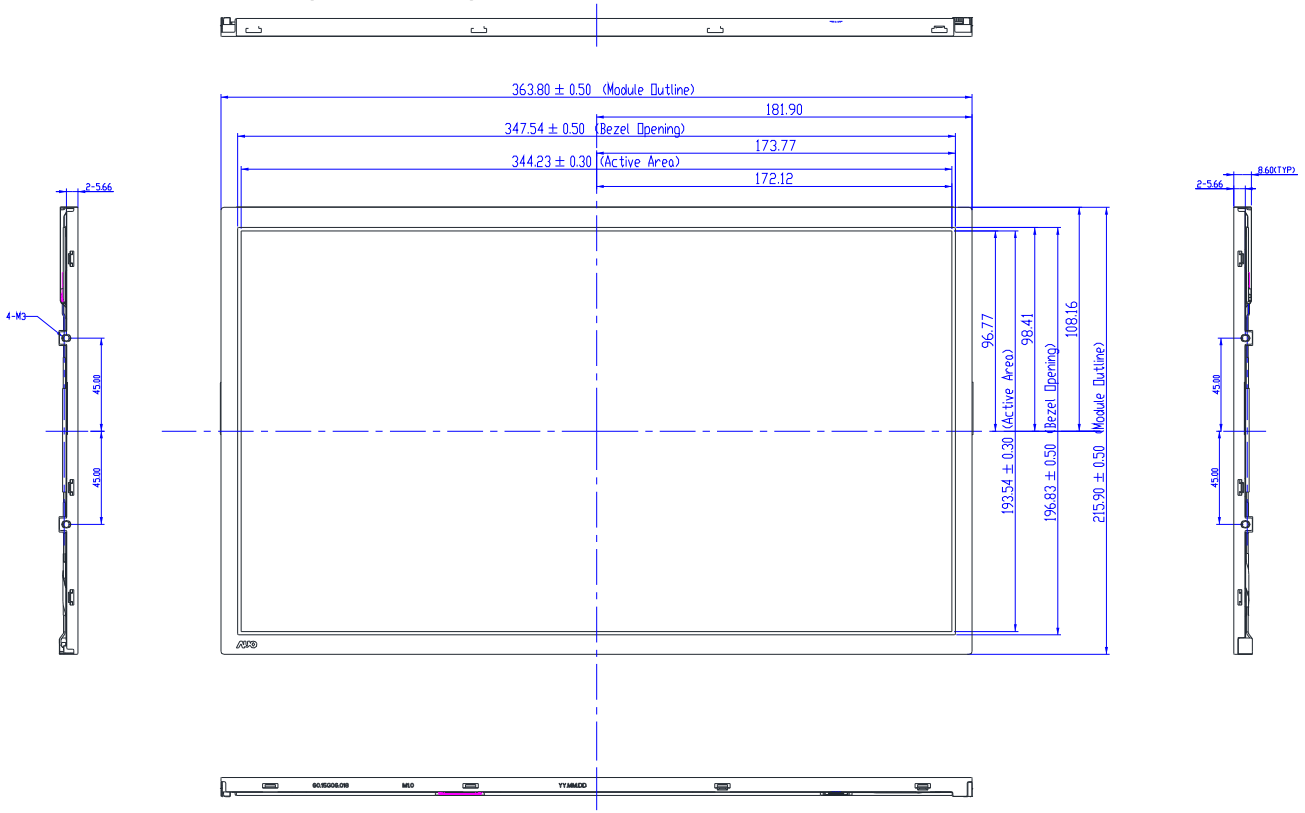
Note 1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Note 2:

- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability. No function failure occurs. Mura shall be ignored after high temperature reliability test.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for
  24 hours at least in advance.

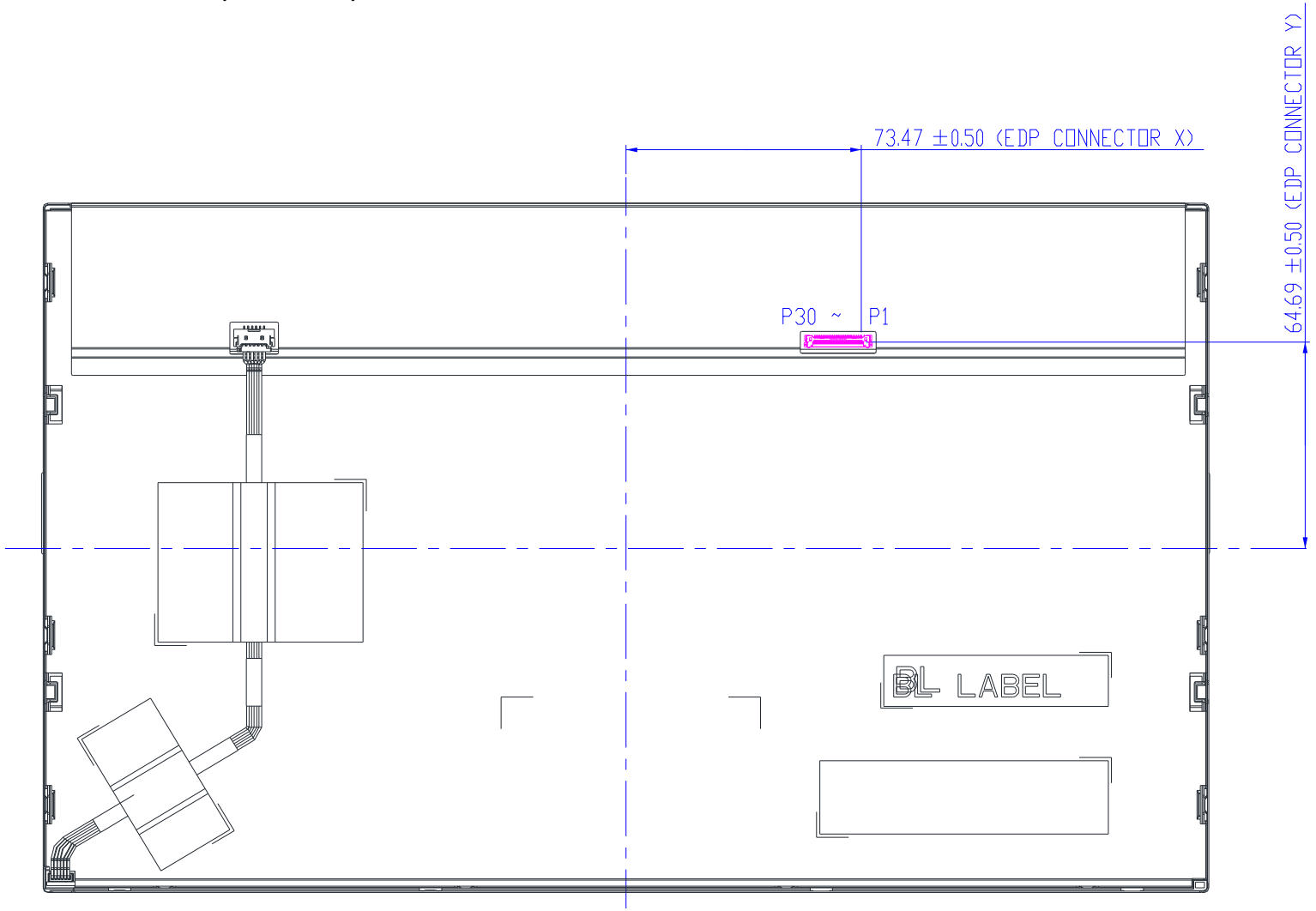
8. Mechanical Characteristics

8.1 LCM Outline Dimension (Front View)



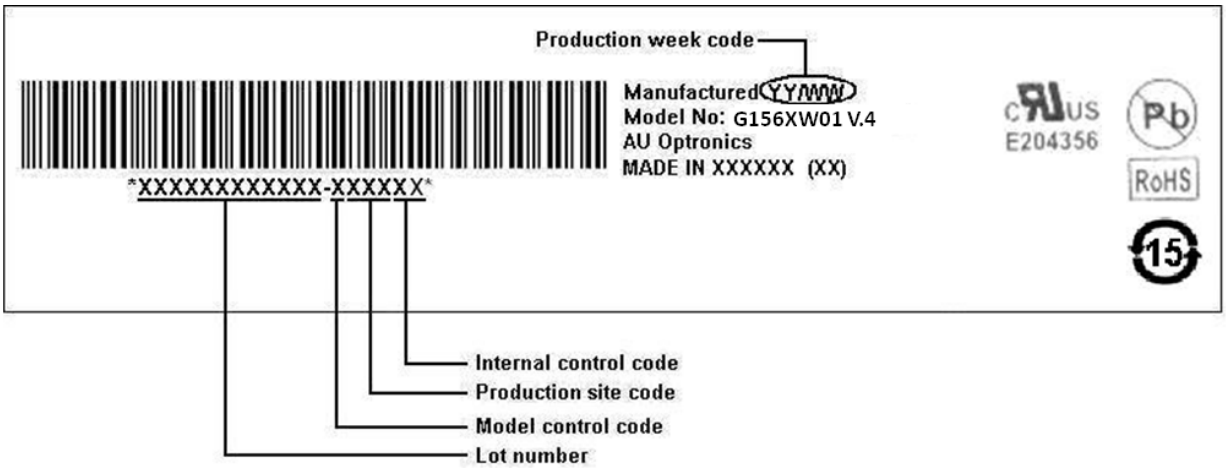
NOTE:
1.PRELIMINARY DRAWING FOR REFERENCE ONLY.
2.TOLERANCE WITHOUT SPECIFIED TO BE 0.5 MM.
3.I/F CONNECTOR: STM MSBKT2407P30HB OR JAE FI-XB30SSL-HF15.
4.THIS DIMENSION EXCLUDES DEFORMATION.
5.TORQUE OF M3 USER HOLE SHOULD BE WITHIN 4 KGF-CM AND RE-SCREW 10 TIMES.
6.M3 SCREW USER HOLE DP=3.6 MAX SCREW PENATRATION

8.2 LCM Outline Dimension (Rear View)

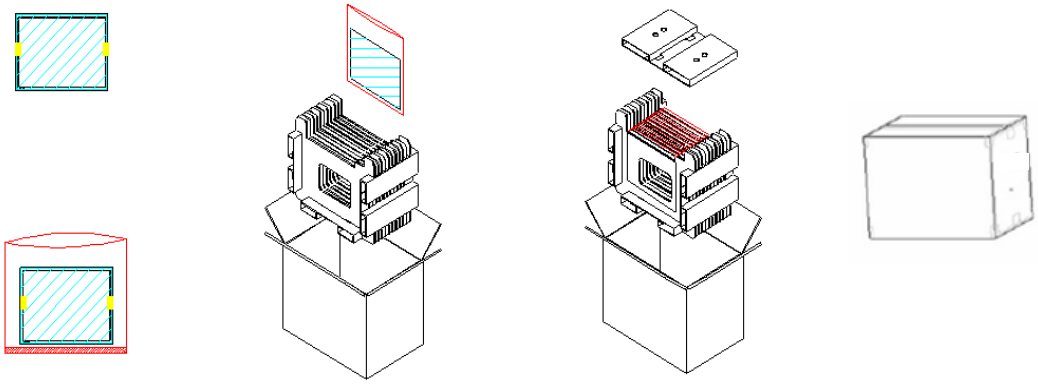


9. Packaging Spec

9.1 Shipping Label (on the rear side of TFT-LCD display)



9.2 Carton & Pallet Package



Max capacity：16 TFT-LCD module per carton

Max weight: 15.3 kg per carton

Outside dimension of carton: 450mm(L)*375mm(W)*319mm(H)

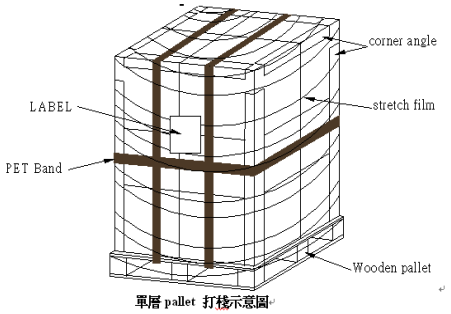
Pallet size： 1150 mm* 910 mm*132mm

Box stacked

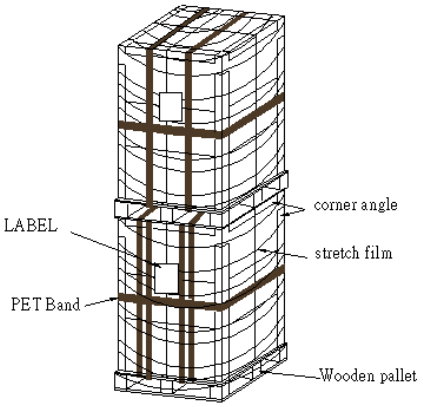
Module by air：(2 *3) *4 layers，one pallet put 24 boxes, total 384pcs module

Module by sea：(2 *3) *4 layers+(2 *3) *1 layers, two pallet put 30 boxes, total 480pcs module

Module by sea_HQ：(2 *3) *4 layers+(2 *3) *2 layers, two pallet put 42 boxes, total 576 pcs module



單層 pallet 打栈示意圖



10. Safety

10.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

10.2 Materials

10.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

10.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process. The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

10.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

10.4 National Test Lab Requirement

The display module will satisfy all requirements for compliance to:

☐ UL 60950-1 second edition U.S.A. Information Technology Equipment

11. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	Define (50)	50	01010000	80	
09	Define (E3)	E3	11100011	227	
0A	Product Code	00	00000000	0	
0B	Product Code	01	00000001	1	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	1B	00011011	27	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	Video input def. (digital I/P, non-TMDS, CRGB)	A5	10100101	165	
15	Max H image size (rounded to cm)	22	00100010	34	
16	Max V image size (rounded to cm)	13	00010011	19	
17	Display Gamma (=(gamma*100)-100)	78	01111000	120	
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	E2	11100010	226	
19	Red/green low bits (Lower 2:2:2:2 bits)	38	00111000	56	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	B5	10110101	181	
1B	Red x (Upper 8 bits)	A0	10100000	160	
1C	Red y/ highER 8 bits	57	01010111	87	
1D	Green x	53	01010011	83	
1E	Green y	9E	10011110	158	
1F	Blue x	27	00100111	39	
20	Blue y	11	00010001	17	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	

25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	12	00010010	18	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active Lower 8bits	56	01010110	86	
39	Horz blanking Lower 8bits	5A	01011010	90	
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	01010000	80	
3B	Vertical Active Lower 8bits	00	00000000	0	
3C	Vertical Blanking Lower 8bits	19	00011001	25	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	36	00110110	54	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	58	01011000	88	
43	Vertical Image Size Lower 8bits	C1	11000001	193	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border (zero for internal LCD)	00	00000000	0	
46	Vertical Border (zero for internal LCD)	00	00000000	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
48	Define	00	00000000	0	
49		00	00000000	0	
4A	Reversed	00	00000000	0	
4B	Panel Vendor Code, 00h: AUO	00	00000000	0	
4C	Reversed	00	00000000	0	
4D	Panel Max Luminance(Typ.)	46	01000110	70	

4E	Reversed	00	00000000	0	
4F	Luminance Control PWM Freq(min)	04	00000100	4	
50	Luminance Control PWM Freq(max)	64	01100100	100	
51	PWM Duty Ratio(min)	02	00000010	2	
52	PWM Duty Ratio(max)	64	01100100	100	
53	Timing T2(max)	14	00010100	20	
54	Timing T3(max)	14	00010100	20	
55	Timing T7(max)	05	00000101	5	
56	Reversed	00	00000000	0	
57	Reversed	00	00000000	0	
58	Reversed	00	00000000	0	
59	Reversed	00	00000000	0	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	47	01000111	71	G
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	35	00110101	53	5
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	58	01011000	88	X
76	Manufacture P/N	57	01010111	87	W

77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	31	00110001	49	1
79	Manufacture P/N	56	01010110	86	V
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	34	00110100	52	4
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	5F	01011111	95	